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09/750,465	12/28/2000	Calvin Guey	JCLA6707	6593

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EXAMINER	
GOLE, AMOL V	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/750,465	GUEY ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

#6: Amendment A (2/12/04)

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of the address calculator being able to generate the address signal according to the decode information in claim 2 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. The Office suggests the applicant to show a connection between the decode information and the address calculator in fig. 1. Also, it would be useful to show a connection between the decode information and the register identification number generator in fig. 1because the register identification number generator uses the decode information.

4. The Office acknowledges and approves the changes to fig. 1 requested on 2/12/04.

5. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 4 is objected to because of the following informalities: On examining claim 4 again, the request for replacing the words "linking up" with "mapping" in the First Office Action seems to be impertinent. The Office requests the applicant to change the wording back to "linking up". The Office regrets any inconvenience caused to the applicant due to this requested change. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim **4, 5 and 6** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 4 recites the limitation "the plurality of registers" in line 7 and the limitation "the memory unit" in line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless –*
>
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

11. Claims **4 and 6** are rejected under 35 U.S.C. 102(b) as being anticipated by Higaki et al. (US005796970A).

[Interpretation 1: The step of "adding the N bits together to form an initial count value" in independent claim 4 is being interpreted here as adding the N bits together in any way including adding some of the bit values directly and some of the bit values multiplied by a constant.]

12. In regard to Claim 4:

13. Higaki et al. disclose a method of executing a block data transfer instruction ("MOVEM" instruction, col. 1, line 28) inside a processor (col. 1, line 33) after receiving decode information (Fig. 4, Register Designating field) containing N bits (Fig. 2, shows the register designating field with 8 bits; col. 1, line 62, indicates that the field can be of N bits), comprising the steps of:

adding (Fig. 4, element 214, number of register detection circuit; Fig. 6D shows a truth table for the circuit which indicates that it performs adding) the N bits together to form an initial count value (Fig. 6D, output column 1; col. 7, line 65-66);

generating a plurality of register identification number (a register identification number generator, Fig. 4, 202, 204) identical in number to the initial count value, wherein the register identification number corresponds to the bit position of the N-bit decode information that has a bit value '1'(col. 6, lines 4-8, 36-50);

mapping the plurality of registers that correspond to the register identification numbers to the memory unit according to the register identification numbers (the instruction decoder Fig. 3, 101, col. 5, lines 17-22, controls the transfer of data between the registers that correspond to the register identification numbers which are successively output by the register designating field decoder, 105, and the memory 104 wherein the address calculator, Fig. 3, 103, col. 5, lines 32-39, successively calculates memory addresses each time register data is transferred based on the control by the instruction decoder) so that stored data can be exchanged between memory unit and the registers.

14. In regard to Claim 6:

15. Higaki et al. further disclose a method which includes generating an address signal (calculator group, Fig. 3, 103, col. 5, lines 27-39) according to the decode information so that stored data in the register corresponding to the register identification number and data within the memory unit having an address corresponding to the address signal can exchange with each other.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

17. Claims **1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Higaki et al. (US005796970A) in view of Brown (US003634658) and Mitsuhira et al. (US005561816A).

18. In regard to claim 1:

19. Higaki et al. disclose an apparatus (col. 1, line 47) for executing block data transfer instruction ("MOVEM" instruction, col. 1, line 28) inside a processor (col. 1, line 33) after receiving decode information (Fig. 4, Register Designating field) containing N bits (Fig. 2, shows the register designating field containing 6 bits designating registers R10-15), the apparatus comprising:

a register identification number generator (Fig. 4, 202, 204) that generates a plurality of register identification numbers (Fig. 4, d) equal in number to the initial count value (Fig. 6D, output column 1; col. 7, lines 65-66), wherein the register identification number corresponds to the bit positions in the N-bit decode information having a bit value '1' (col. 6, lines 4-8, 36-50);

a memory unit (Fig. 3, 104, col. 5, lines 40-41) for holding data; and

a register list (Fig. 3, 102) that includes a plurality of registers (col. 5, lines 23-24), wherein the register list is able to receive the register identification numbers (Fig. 3, output of 105) so that the stored data can be freely exchanged between the memory unit and the registers that correspond to the register identification numbers.

20. The apparatus disclosed by Higaki et al., although shows a number of registers detection circuit 214 which outputs the initial count value using the bits in the register designating field (col. 7, lines 54+) it differs from the present invention because it does not expressly disclose an **adder** for receiving the N-bit decode information and adding the N bits together to produce an initial count value and a **counter** for receiving the initial count value, which decreases the value by one after outputting a count control signal.

21. Brown teaches that an adder (fig. 3, four bit counter 20) can be used to add the input bits together to produce a count value indicating the number of bits set. Its truth table is shown in table B in col. 2. Brown teaches that the parallel bit counter is faster

than simple serial shift counters (col. 1, lines 7-20, 27-30) indicating its usefulness in systems where faster performance is important.

22. Mitsuhira et al. teach a down counter (fig. 6, DC 131) in a DMA transfer mechanism in which DC 131 holds the number of data to be transferred (col. 6, lines 7-10) and decrementer 130 decrements the value of DC by one after each DMA transfer (col. 8, lines 17-20). When DC is equal to zero, the data transfer is completed and a DC-zero detecting signal 151 is activated to indicate this and initiate the next transfer (col. 8, lines 30-34).

23. In light of the Brown reference one of ordinary skill in the art would have recognized that an adder circuit could be used in the number of registers detection circuit 214 to add bits 2-7 designating registers R15-R10 to generate the initial count value when bit 1 is 0. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have implemented the registers detection circuit 214 with an adder as taught by Brown to generate the initial count value. One would have been motivated to do so because Brown teaches that the adder circuit is fast and hence would aid in improving performance (col. 1, lines 7-20, 27-30).

24. Higaki et al. disclose that the outputs of the priority encoder 202, e, and the group processing continuation signal generation circuit 210, h, are inputted to the register processing completion detection circuit 211 to generate a register processing continuation signal which is set to a "1" (valid) indicating that the registers designated to be transferred are being processed (fig. 4; col. 7, lines 44-47). One of ordinary skill in the art would have recognized that one could simplify the Higaki et al. circuit by

replacing the circuitry within the priority encoder circuit that generates the bit detection continuation signal e, the group processing continuation signal generation circuit 210, and the register processing completion detection circuit 211 with a down counter which counts down from the initial count value already calculated by the number of registers detection circuit 214 to indicate that register processing is continuing and when it reaches zero, indicate that the transfer is complete similar to Mitsuhira et al. Therefore it would have been obvious to one of ordinary skill in the art to have modified the Higaki et al. invention by using a simple down counter to generate the register processing continuation signal. One would have been motivated to do so because it would lead to hardware savings and hence savings in cost.

25. In regard to Claim 2:

26. Higaki et al. teach an address calculator (Fig. 3, 103, col. 5, lines 27-39) for generating an address signal according to the decode information and then outputting the address signal to the memory unit (fig. 3, memory 104) so that data can be freely exchanged between the registers that correspond to the register identification numbers and the addressed memory in the memory unit according to the address signal.

27. Claim **3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Higaki et al. (US005796970A) in view of Brown (US003634658) and Mitsuhira et al. (US005561816A) as applied to claim 1 above, and further in view of McAlister et al. (US004348741).

28. In regard to claim 3:

29. The combination of Higaki et al. in view of Brown and Mitsuhira et al. teaches that the register identification number generator (Fig. 4, 202 [priority encoder], 204) for generating register identification numbers equal in number to the initial count value, is able to generate corresponding register identification number according to the bit position (col. 6, lines 36-39) in the N-bit (Fig. 2, shows the register designating field containing 6 bits designating registers R10-15) decode information that has a value '1' (col. 6, lines 4-8).

30. Higaki et al. only provide a truth table for the priority encoder in fig. 6A but do not teach that the register identification number generator includes N logic units and that when the counter decrements by one down to zero, the N logic unit is able to generate the corresponding register identification number according to the bit position in the N-bit decode information that has a value one.

31. McAlister et al. teach a priority encoder which is simple, fast, and occupies less space on chip (col. 2, lines 35-37). It has 16 units (Fig. 2) for a 16-bit input.

32. Higaki et al. use a priority encoder 202 for register transfer processing. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the

invention to have used the priority encoder circuitry taught by McAlister to implement the priority encoder 202 of Higaki et al. because it is simple, fast, and conserves space providing the benefits of better performance and lower costs.

33. The combination of Higaki et al. in view of Brown and Mitsuhira et al. teaches that counter counts down to zero as each register is processed and that the priority encoder generates the bit position number for each bit position with a value of one to indicate the register identification number (Higaki: fig. 6A; col. 6, lines 4-19). Therefore, in the combination in view of McAlister, the N logic unit would generate the bit position number for each bit position with a value of one to indicate the register identification number when the counter counts down to zero.

34. Claims **4 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Higaki et al. (US005796970A) in view of Brown (US003634658).

[Interpretation 2: The step of "adding the N bits together to form an initial count value" in independent claim 4 is being interpreted here as doing a linear addition of the N bits wherein the value of each bit position corresponding to the N bits is added once to generate the initial count value.]

35. In regard to claim 4:

36. A method of executing block data transfer instruction ("MOVEM" instruction, col. 1, line 28) inside a processor (col. 1, line 33) after receiving an N-bit decode information (Fig. 4, Register Designating field containing 6 bits designating registers R10-15), comprising the steps of:

generating a plurality of register identification number (Fig. 4, 202, 204) identical in number to the initial count value (Fig. 6D, output column 1; col. 7, lines 65-66), wherein the register identification number corresponds to the bit position of the N-bit decode information that has a bit value `1` (col. 6, lines 4-8, 36-50); and

mapping the plurality of registers that correspond to the register identification numbers to the memory unit according to the register identification numbers so that stored data can be exchanged between the memory unit and the registers (the instruction decoder Fig. 3, 101, col. 5, lines 17-22, controls the transfer of data between the registers that correspond to the register identification numbers which are

successively output by the register designating field decoder, 105, and the memory 104 wherein the address calculator, Fig. 3, 103, col. 5, lines 32-39, successively calculates memory addresses each time register data is transferred based on the control by the instruction decoder).

37. The method disclosed by Higaki et al., although shows the usage of a number of registers detection circuit 214 to output the initial count value using the bits in the register designating field (col. 7, lines 54+), differs from the present invention because it does not disclose the step of adding the N bits together to form an initial count value.

38. Brown teaches that an adder (fig. 3, four bit counter 20) can be used to add the input bits together to produce a count value indicating the number of bits set. Its truth table is shown in table B in col. 2. Brown teaches that the parallel bit counter is faster than simple serial shift counters (col. 1, lines 7-20, 27-30).

39. In light of the Brown reference one of ordinary skill in the art would have recognized that an adder circuit could be used to add bits 2-7 designating registers R15-R10 to generate the initial count value when bit 1 is 0. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have implemented the registers detection circuit 214 with an adder as taught by Brown to generate the initial count value. One would have been motivated to do so because Brown teaches that the adder circuit is an efficient design and can lead to lower costs (col. 1, lines 7-20, 27-30).

40. In regard to claim 6:

41. Higaki et al. further disclose a method which includes generating an address signal (calculator group, Fig. 3, 103, col. 5, lines 27-39) according to the decode information so that stored data in the register corresponding to the register identification number and data within the memory unit having an address corresponding to the address signal can exchange with each other.

42. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Higaki et al. (US005796970A) in view of Brown (US003634658) as applied to claim 4 above, and further in view of Mitsuhira et al. (US005561816A).

43. In regard to Claim 5:

44. Higaki et al. further teach a method wherein the step for generating the register identification numbers includes the sub-step of generating a register identification number whenever a bit value '1' is found in the N-bit decode information (col. 6, lines 4-8, 36-39).

45. The method taught by Higaki et al. differs from the present invention because it does not disclose performing a count down operation decreasing the initial value count by one until the value zero is reached and of generating the register identification number after each count down operation.

46. Mitsuhira et al. teach a down counter (fig. 6, DC 131) in a DMA transfer mechanism in which DC 131 holds the number of data to be transferred (col. 6, lines 7-

10) and decrementer 130 decrements the value of DC by one after each DMA transfer (col. 8, lines 17-20). When DC is equal to zero, the data transfer is completed and a DC-zero detecting signal 151 is activated to indicate this and initiate the next transfer (col. 8, lines 30-34).

47. Higaki et al. disclose that the outputs of the priority encoder 202, e, and the group processing continuation signal generation circuit 210, h, are inputted to the register processing completion detection circuit 211 to generate a register processing continuation signal which is set to a "1" (valid) indicating that the registers designated to be transferred are being processed (fig. 4; col. 7, lines 44-47). One of ordinary skill in the art would have recognized that one could simplify the Higaki et al. circuit by replacing the circuitry within the priority encoder circuit that generates the bit detection continuation signal e, the group processing continuation signal generation circuit 210, and the register processing completion detection circuit 211 with a down counter which counts down from the initial count value already calculated by the number of registers detection circuit 214 to indicate that register processing is continuing and when it reaches zero, indicate that the transfer is complete similar to Mitsuhira et al. Therefore it would have been obvious to one of ordinary skill in the art to have modified the Higaki et al. invention by using a simple down counter to generate the register processing continuation signal. One would have been motivated to do so because it would lead to hardware savings and hence savings in cost.

48. Also the combination of Higaki et al. in view of Brown and Mitsuhira et al. inherently teaches that after every count down operation the register number would be generated because the count down operation indicates the transfer of a register.

Response to Amendment

49. Applicant's arguments filed on 2/12/04, paper number 6, have been fully considered.

50. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

51. The arguments with regard to the 35 USC 102 rejections are not persuasive. On pages 5 and 6 Applicant argues in essence:

> *" Higaki does not disclose the feature of "... adding the N bits together to form an initial count value;" as claimed in claim 4."*

52. However Higaki teaches that the function of adding is performed by the number of registers detection circuit 214 as can be seen from its truth table in fig. 6D. For example when 3 bits are valid, the output is 3, which is the addition of 3 valid bits. When 6 bits are valid, the output is 6, which is the addition of 6 valid bits. In the case when the bit specifying the group of 10 registers is set, the circuit performs the function of adding the bit values of the 6 bits 2-7 and then adding the bit value of the bit 1 multiplied by 10 or adding the bit value of bit 1, ten times. So effectively, the function of adding the N bits

together in way or another is performed. The claim does not limit adding the N bits together in any way.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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